Claims

1. A planar lightwave circuit, comprising:

at least one optical waveguide core;

at least one feature proximate the core having at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core; and

a protective passivation layer formed over the core and the feature, the passivation layer formed to be substantially non-interfering with the balanced stress affecting the core provided by the feature.

2. The planar lightwave circuit of claim 1, wherein the at least one feature comprises an overcladding layer formed over the core, and doped to balance stress affecting the core.

3. The planar lightwave circuit of claim 2, further comprising:

a substrate; and

an undercladding formed over the substrate and under the core;

wherein the overcladding is doped to have a coefficient of thermal expansion approximately matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core.

4. The planar lightwave circuit of claim 3, wherein the protective passivation layer is formed to have a coefficient of thermal expansion approximately matched to that of the overcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overcladding.

5. The planar lightwave circuit of claim 4, wherein the passivation layer comprises silicon nitride.

6. The planar lightwave circuit of claim 4, wherein the at least one feature comprises portions of the undercladding, respectively adjacent to each lower edge of the core, terminating at a point lower than the core, to further effect a removal of stress away from the core.

7. The planar lightwave circuit of claim 4, wherein the at least one feature comprises a stress release groove formed through the overcladding between two cores of the at least one core, the stress release groove releasing and therefore balancing stress affecting the two cores.

8. The planar lightwave circuit of claim 7, wherein a second overcladding is formed along walls and a floor of the stress release groove to partially but not completely fill the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

9. The planar lightwave circuit of claim 7, wherein the at least one feature comprises portions of the undercladding, respectively adjacent to opposing lower edges of each core, terminating at a point lower than the cores, to further effect a removal of stress away from the cores.

10. The planar lightwave circuit of claim 9, wherein the lower point corresponds with the bottom of the stress release groove to thereby provide an identifiable etch transition point for the stress release groove.

11. The planar lightwave circuit of claim 1, wherein the at least one feature comprises a stress release groove formed through overcladding between two cores of the at least one core, the stress release groove releasing and therefore balancing stress affecting the two cores.

12. The planar lightwave circuit of claim 11, wherein a second overcladding is formed along walls and floor of the stress release groove to partially but not completely fill the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

13. The planar lightwave circuit of claim 1, wherein the at least one feature comprises portions of an undercladding, respectively adjacent to each lower edge of the core, terminating at a point lower than the core, to further effect a removal of stress away from the core.

14. A method for forming a planar lightwave circuit, comprising:

forming at least one optical waveguide core;

forming at least one feature proximate the core having at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core; and

forming a protective passivation layer over the core and the feature, the passivation layer formed to be substantially non-interfering with the balanced stress affecting the core provided by the feature.

15. The method of claim 14, wherein said forming the at least one feature comprises:

forming an overcladding layer over the core; and

doping the overcladdding to balance stress affecting the core.

16. The method of claim 15, further comprising:

providing a substrate and an undercladding formed over the substrate, over which the core is formed;

wherein the overcladding is doped to have a coefficient of thermal expansion approximately matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core.

17. The method of claim 16, wherein said forming the protective passivation layer comprises:

forming the layer to have a coefficient of thermal expansion approximately matched to that of the overcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overcladding.

18. The method of claim 17, wherein the passivation layer comprises silicon nitride.

19. The method of claim 17, wherein said forming the at least one feature comprises:

removing portions of the undercladding, respectively adjacent to each lower edge of the core, to a point lower than the core, to further effect a removal of stress away from the core.

20. The method of claim 17, wherein said forming the at least one feature comprises:

forming a stress release groove through the overcladding between two cores of the at least one core, the stress release groove releasing and therefore balancing stress affecting the two cores.

21. The method of claim 20, further comprising:

forming a second overcladding along walls and floor of the stress release groove to partially but not completely fill the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

22. The method of claim 20, wherein said forming the at least one feature comprises:

removing portions of the undercladding, respectively adjacent to opposing lower edges of each core, to a point lower than the cores, to further effect a removal of stress away from the cores.

23. The method of claim 22, wherein the lower point corresponds with the desired bottom of the stress release groove, the method further comprising:

using the lower point as an identifiable etch transition point for the stress release groove while forming the stress release groove.

24. The method of claim 14, wherein said forming the at least one feature comprises:

forming a stress release groove through overcladding between two cores of the at least one core, the stress release groove releasing and therefore balancing stress affecting the two cores.

25. The method of claim 24, further comprising:

forming a second overcladding along walls and floor of the stress release groove to partially but not completely fill the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

26. The method of claim 14, wherein said forming the at least one feature comprises:

removing portions of an undercladding, respectively adjacent to each lower edge of the core, to a point lower than the core, to further effect a removal of stress away from the core.

27. A method for protecting, and balancing stress in, a planar lightwave circuit having at least one optical waveguide core, comprising:

using at least one feature proximate the core embodying at least one stress-engineered property to balance stress and therefore minimize birefringence affecting the core; and

using a protective passivation layer over the core and the feature, the passivation layer formed to be substantially non-interfering with the balanced stress affecting the core provided by the feature.

28. The method of claim 27, wherein said using the feature includes:

using an overcladding layer over the core, doped to balance stress affecting the core.

29. The method of claim 28, wherein the circuit includes a substrate and an undercladding formed over the substrate, over which the core is formed; and

wherein the overcladding is doped to have a coefficient of thermal expansion approximately matched to that of the substrate to thereby symmetrically distribute stress in the undercladding between the overcladding and the substrate, and therefore away from the core.

30. The method of claim 29, wherein the passivation layer has a coefficient of thermal expansion approximately matched to that of the overcladding such that it is substantially non-interfering with the balanced stress affecting the core provided by the overcladding.

31. The method of claim 30, wherein the passivation layer comprises silicon nitride.

32. The method of claim 30, wherein said using the feature includes:

using portions of the undercladding, respectively adjacent to each lower edge of the core, which terminate at a point lower than the core, to further effect a removal of the stress away from the core.

33. The method of claim 30, wherein said using the feature includes:

using a stress release groove formed through the overcladding between two cores of the at least one core, the stress release groove releasing and therefore balancing stress affecting the two cores.

34. The method of claim 33, further comprising:

using a second overcladding along walls and floor of the stress release groove partially but not completely filling the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

35. The method of claim 33, wherein said using the feature includes:

using portions of the undercladding, respectively adjacent to opposing lower edges of each core, which terminate at a point lower than the cores, to further effect a removal of stress away from the cores.

36. The method of claim 35, wherein the lower point corresponds with the desired bottom of the stress release groove, to thereby serve as an identifiable etch transition point for the stress release groove.

37. The method of claim 27, wherein said using the feature includes:

using a stress release groove through overcladding between two cores of the at least one core, the stress release groove releasing and therefore balancing stress affecting the two cores.

38. The method of claim 37, further comprising:

using a second overcladding along walls and floor of the stress release groove to partially but not completely fill the groove to preserve its stress releasing property, but sufficient to support a generally planar portion of the passivation layer over the groove.

39. The method of claim 27, wherein said using the feature includes:

using portions of an undercladding, respectively adjacent to each lower edge of the core, terminating at a point lower than the core, to further effect a removal of the stress away from the core.

40. A planar lightwave circuit having a depth-controlled stress release groove, comprising:

at least two waveguide cores formed between an undercladding layer and an overcladding layer, the undercladding layer between the two cores terminating at a point lower than the lower surfaces of the two cores; and

a stress release groove formed through the overcladding between the two cores to a depth corresponding to the lower point.

41. A method for forming a stress release groove in a planar lightwave circuit, comprising:

providing a substrate and a waveguide undercladding formed thereover;

forming a waveguide core material layer over the undercladding;

etching portions of the waveguide core material away to form at least two waveguide cores, said etching proceeding into the undercladding between the two cores, to a point lower than the lower surfaces of the cores;

filling the etched portions with a waveguide overcladding; and

etching the stress release groove through the overcladding between the cores, and to the lower point, including sensing the lower point as an etch transition point.

42. A planar lightwave circuit, comprising:

at least two waveguide cores formed over an undercladding layer, the portion of the undercladding layer between the two cores terminating at a point lower than the lower surfaces of the cores to relieve stress and resulting birefringence from the cores; and

an overcladding formed over the undercladding between the two cores.

43. The planar lightwave circuit of claim 42, wherein the distance between the point and the lower surfaces of the cores is proportional to the amount of stress relieved from the cores.

44. A method for forming a planar lightwave circuit, comprising:

providing a substrate and a waveguide undercladding formed thereover;

forming a waveguide core material layer over the undercladding;

etching portions of the waveguide core material away to form at least two waveguide cores, said etching proceeding into the undercladding between the two cores, to a point lower than the lower surfaces of the cores;

filling the etched portions with a waveguide overcladding;

wherein the lower point of the undercladding between the cores relieves stress and resulting birefringence from the cores.

45. The method of claim 44, wherein the distance between the point and the lower surfaces of the cores is proportional to the amount of stress relieved from the cores